Self-driven Constant Voltage Reset Circuit

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Abstract—**This paper presents a reset mechanism, which combines the advantages of the active clamp reset and the traditional third wire reset technique. In this concept the reset voltage is constant similar to the third wire reset, wherein a constant voltage is applied to the transformer during the reset cycle. The technology has several key advantages from the active clamp reset mechanism. The energy contained in the leakage and magnetizing inductance is recycled, and the voltage across the main switch is clamped. In addition to this, the flux trough the transformer is symmetrical to zero and the duty cycle can be higher than 50%, similar to the active clamp circuit. Though this circuit contains most of the active clamp circuit' key features it does not exhibit its limitations. One of the drawbacks of the active clamp circuit is its behavior during transients wherein the duty cycle changes. During transients, until the reset capacitor charges to its optimum level, the voltage across the switch may reach uncontrollable levels. In this reset technique the voltage across the switch is constant regardless of the duty cycle and reacts to transients without any limitations. In additional to this the implementation is very simple; it does not require any additional driving and timing circuits for the reset switch. The reset switch is driven directly form the transformer by a driving winding and the reset voltage can be easily adjusted by a resistor divider. Using this technology a DC-DC Converter was implemented, providing 1.2V @ 20A, from an input voltage range of 36V to 60 reaching an efficiency of 86% at full load.**

I. INTRODUCTION

The increasing demand for distributed power systems, lead to a focus in the implementation of a high efficiency, high power density, board mounted DC-DC converters.

The continuous decrease of the output voltage requirements from (3.3V, 1.5V, 1.2V, 0.8V etc.) and increased output current has placed more challenges on the power designer.

The task becomes even more challenging for low power (less than 25W) high efficiency converters, wherein high power density is required. The lack of space requires a simple configuration with reduced number of parts in the power train section and the control as well. The forward topology is highly suitable in applications, which require high current and low output voltages. The forward topology requires a reset circuit, which can be implemented in many different ways. The traditional technique is using an additional reset winding and a reset diode as depicted in figure 1. By tailoring the turn ratio between the reset winding and the primary winding, N1/N2 the reset voltage can be controlled. In this application the leakage inductance energy is only partially recovered, which is a function of the coupling between the reset winding and the power train windings. A snubber or a clamp circuit may also be needed to limit the voltage spikes across the primary switch. The flux in the transformer swings between Br and the peak flux value for the first cycle and after that, its level during the dead time may change function of the reverse current through the primary winding caused by the resonance between L1 and parasitic capacitance of Q1. The active clamp reset circuit has gained popularity in 1990s due to some key advantages. The concept [1] and depicted in figure 2 requires an additional reset switch in series with a reset capacitor, the circuit can be placed in parallel with the primary winding or across the main switch. The reset switch is turned on during the turn off time of the main switch. The resonant frequency between the reset capacitor and the primary inductance is chosen to be several times smaller than the switching frequency and as a result, the voltage across the resonant capacitor is not changing during the steady state operation. The voltage across the reset capacitor is Vin/(1-D). This circuit offers optimum reset due to the fact that the reset time occurs during the entire off time period of the main switch. As a result, the voltage across the primary switch is minimized, the duty cycle can be larger than 50%, and the flux in the transformer is symmetrical to zero. In addition, the leakage inductance and magnetizing inductance energy is recycled and the voltage across the primary switch is clamped. This long list of advantages made this topology very popular in the last ten years. However, there are several limitations associated with it, which limits its applications when fast dynamic are required. During transients, until the reset capacitor charges to its optimum level, the voltage across the switch may reach very high levels. To protect the main switch additional circuits such as maximum volt-second circuits are necessary. This protection circuit in addition to the timing and driving circuit for the reset switch complicates the control section. A complexity not justified for power levels under 25W. To maintain the simplicity of the circuit in applications of this power level, resonant reset has been often used. In the resonant reset, a capacitor is placed across the main switch. When the main switch turns off the inductance of the primary winding resonates with the resonant capacitor and the output

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capacitor of the main switch. The flux through the transformer is symmetrical to zero and the voltage stress on the switch is a function of the elements of the resonant circuit. Some tradeoff applies between the voltage stress on the main switch and the switching losses, especially due to the limited flexibility for the primary winding inductance. The goal is to have a reset mechanism, which offers the simplicity of the resonant reset and the key features of the active clamp reset without its dynamic limitations.

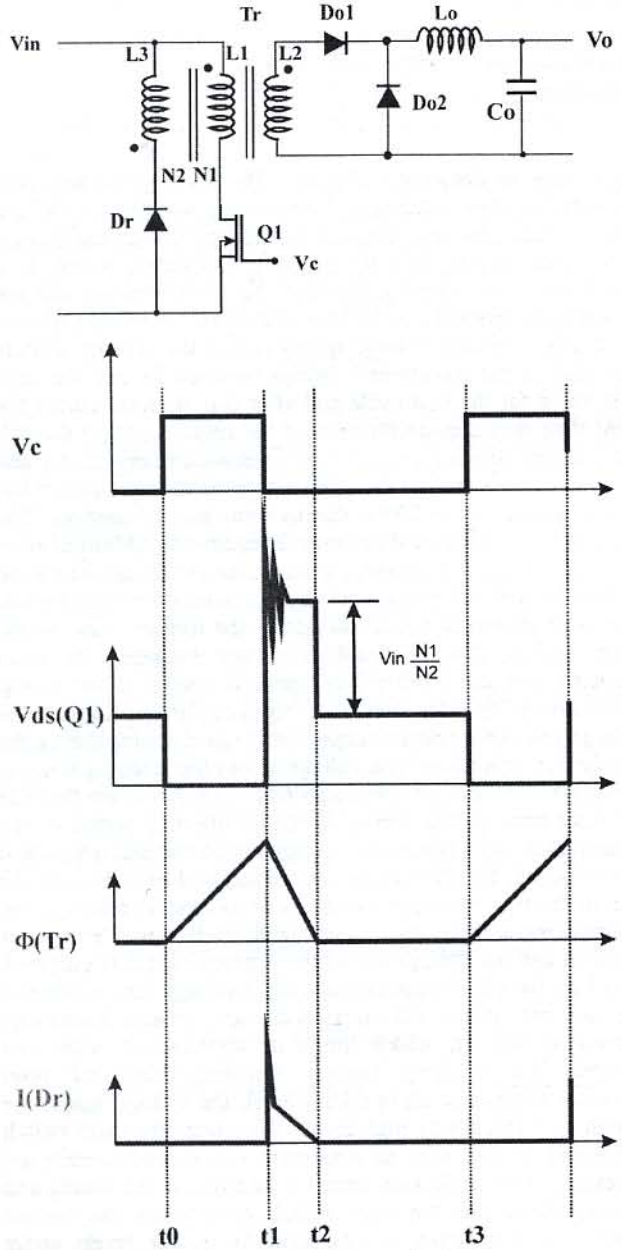

Figure 1. Third wire reset circuit

II. CIRCUIT OPERATION

In figure 1 is presented the simplified schematic and the key waveforms for this reset technique. We identified four stages of operation

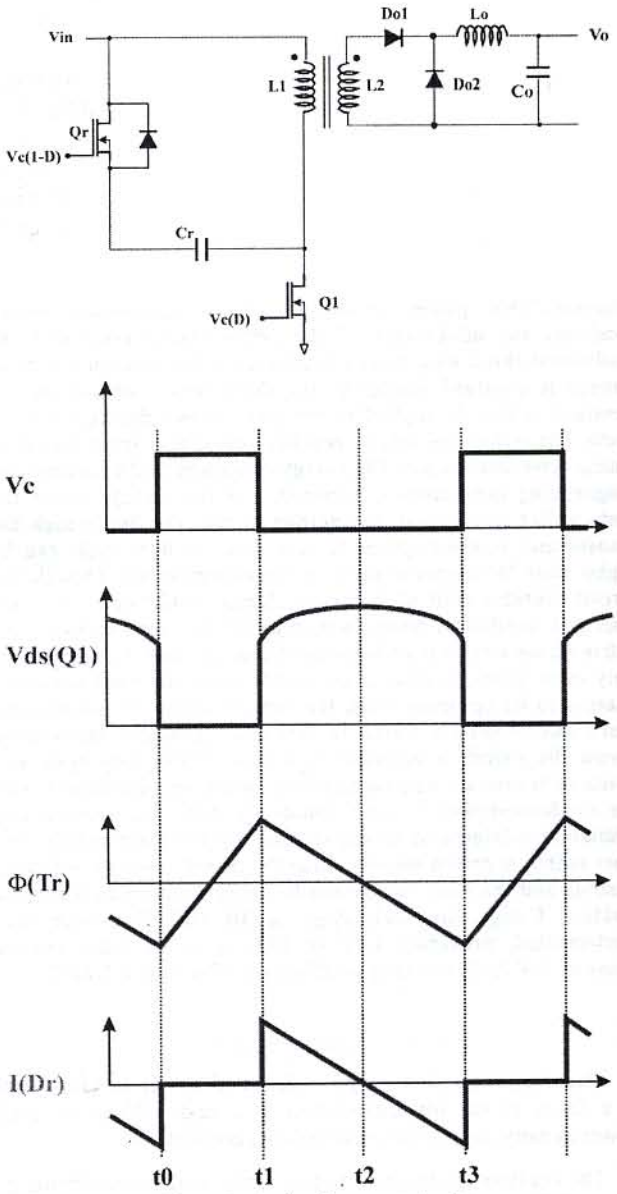

Figure 2. Active clamp reset circuit

A. STAGE 1 (t0-t1)

At the moment t0, the primary power switch Q1 is turned on and the magnetic flux will build through the transformer while the output rectifier Do1 will turn on and the power will be transferred to the secondary while increasing the storage energy in Lo. For simplicity, the output rectifiers shown are diodes though in the final application we are using synchronized rectifiers.

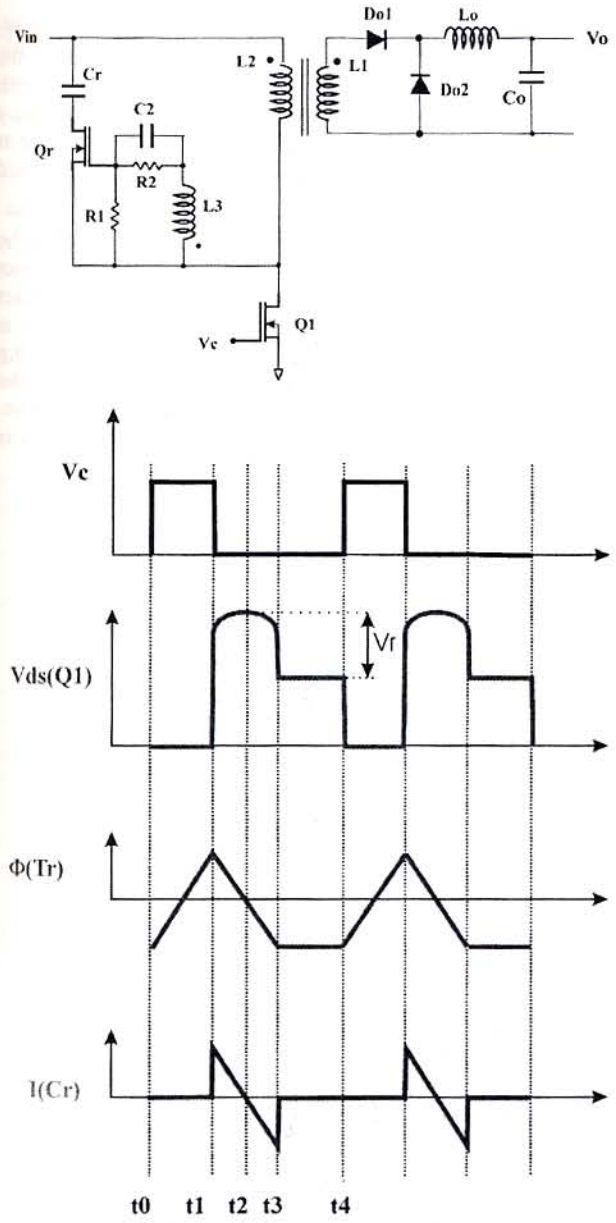

Figure 3. Self-driven constant voltage reset circuit [20]

B. STAGE 2 (t1-t2)

At the moment t1, the main switch Q1 is turned off. The magnetizing current and the leakage current will charge the output capacitance of the main switch and then flow through the body diode of Qr and the capacitor Cr. At the same time in the secondary Do2 will be pushed into conduction and the energy stored in Lo will be further transferred to the load. The voltage polarity will change across L3 and Qr will turn on further reducing the impedance. The magnetizing current will continue to flow charging Cr. The resonant frequency between Cr and the inductance of the primary winding is lower than the switching frequency; as a result, the voltage across Cr will not change during the reset cycle. At this time, the flux in the transformer is pushed back towards zero.

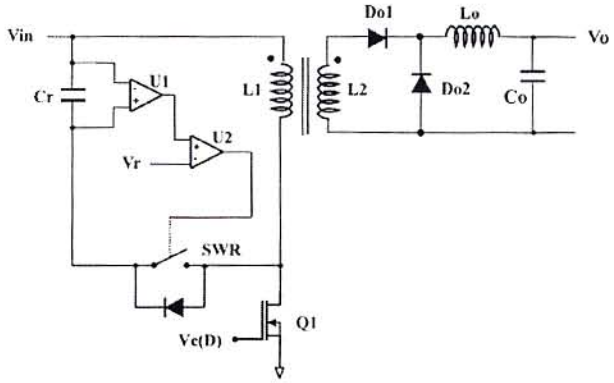

Figure 4. Self-driven constant voltage reset circuit [20]

C. STAGE 3 (t2-t3)

At the moment t2 the current changes direction through the reset switch Qr and start discharging the Cr. The flux through the transformer is also pushed to the negative side. Cr will be further discharged until the voltage in the gate of Qr will reach the turn off threshold. The Qr will start to turn off exhibiting a larger impedance between drain to source and the voltage in L3 will further collapse with a positive feedback until at t3, Q3 is turned off. The reset voltage, Vr is a function of the turns ratio between L2 and L3, the divider ratio R1 and R2, and the characteristic of Qr.

D. STAGE 4 (t3-t4)

At the moment t3, the reset switch Qr is turned off. During this time period, the voltage across the main switch is steady and equal to the input voltage, the flux in the transformer is also steady and in the secondary, Do2 is still conducting transferring the energy from Lo to the load. The presence of the dead time may appear, at first sight, as a major drawback for this reset technique, due to the fact that this time interval is not used for reset and as a consequence the voltage stress on the main switch is higher. This drawback is offset by the capability of this circuit to allow an increase of the duty cycle up to the elimination of the dead time, without changing the voltage across the main switch. It does not have the "reset voltage memory" associated with the traditional active clamp reset, which limits its dynamic performance.

Though in this implementation an additional winding of the transformer is used to obtain and process the information about the reset voltage, this technology can be implemented in many ways. The general concept is depicted in figure 4.

The voltage across the reset winding is compared against a reference voltage during the reset time and if the voltage decreases under the reference level the reset switch SWr turns off. The Vr can be fixed or it can vary with the input voltage in order to emulate more of the features of the active clamp. However, for a good dynamic performance the dead time is absolutely necessary.

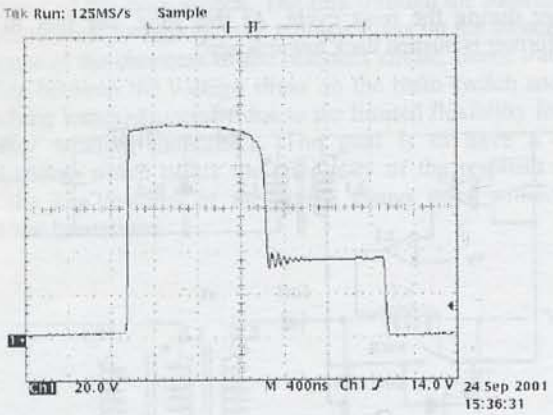

Figure 5. Vds(Q1) Vin=40V, Io=20A, Vo=1.2V

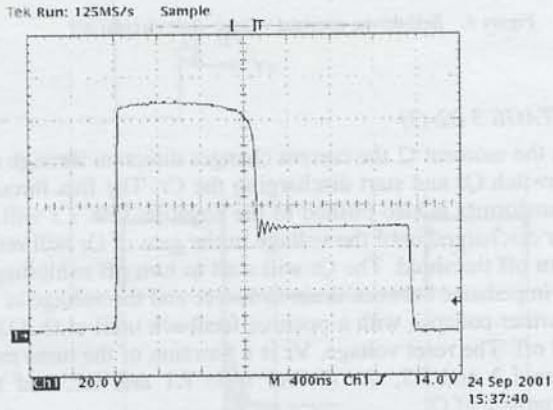

Figure 6. Vds(Q1) Vin=50V, Io=20A, Vo=1.2V

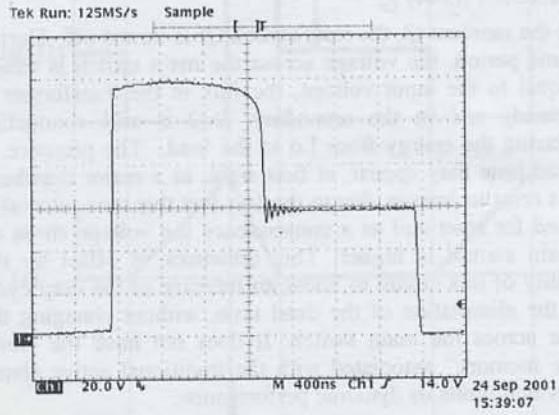

Figure 7. Vds(Q1) Vin=60V, Io=20A, Vo=1.2V

III. EXPERIMENTAL RESULTS

Using this reset technique a 24W, 1.2V @ 20A DC-DC Converter operating from an input voltage of 36V to 60V was built and evaluated. The transformer is using a planar E18 core and the windings are embedded in a 107um (3oz), four layers PCB.

There are 8 turns in primary and one turn in the secondary. This turns ratio was chosen to give to the converter the capability of providing an adjustable output voltage between 0.8 to 1.8V, with a nominal output of 1.2V. The efficiency peaks at 86% at full load. The efficiency versus load curve at nominal input voltage and nominal output voltage is presented in figure 8.

In Figure 5, Figure 6 and Figure 7 are presented the voltages across the main switch for three different input voltages. From these waveforms, it can be noticed that the reset voltage is constant. The voltage stress on the main switch is Vds(Q1)=Vin+Vr. In this application Vr=60V. During transients when the duty cycle changes the voltage stress on the main switch does not change as long as there is a dead time. The voltage rating for the reset switch and the main switch is 150V.

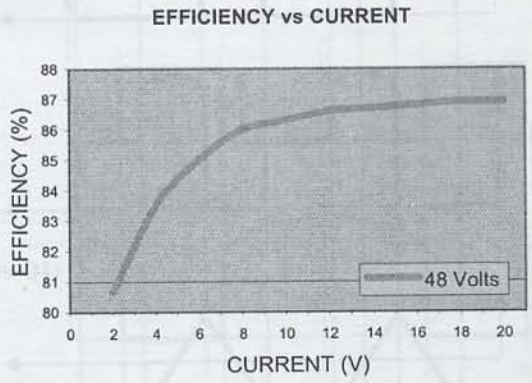

Figure 8. Efficiency versus load

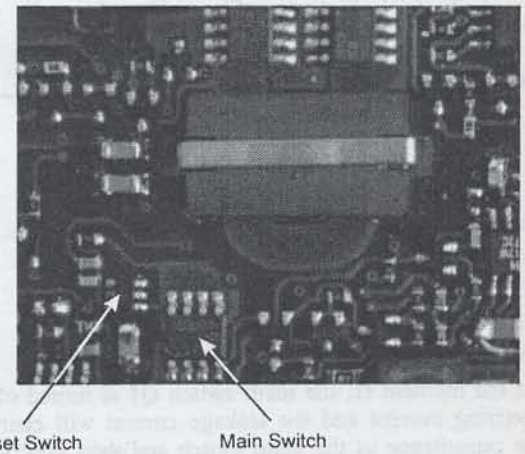

Figure 9. Self-driven constant voltage reset circuit implementation

In figure 9 is depicted the implementation of this converter. The main switch and the reset switch are marked. The key advantage of this concept is its simplicity. The driving circuit of the reset switch is reduced to a one-turn winding, two resistors, and a capacitor. There is no need for a timing circuit to derive the reset drive signal, and there is no need for a

maximum volt second circuit, and there is no need for a driving circuit for the reset switch. The operation frequency of the converter is approximately 300Khz.

IV. CONCLUSION

The proposed circuit technique offers the following advantages:

- The leakage and magnetizing inductance energy is recycled.
- The voltage across the main switch is clamped. The energy contained in the parasitic inductive elements of the transformer and layout is recycled through the reset capacitor.
- The flux through the transformer is symmetrical to zero and as a result, there is a better utilization of BH curve. This symmetry is also maintained during transients unlike the optimum reset technique, because the reset of the transformer is done at each cycle. As a result, the sizing of the magnetic core can be optimized without the necessary margin allowing for transients.
- During transients when the duty cycle changes, the voltage across the primary switchers is constant. A simple resistor divider can easily set the reset voltage.
- It is a very simple circuit, which does not require special timing, volt- second clamp or driving circuit for the reset switch. It combines the simplicity of the resonant reset with the key advantages of the optimum reset without its main disadvantage, the transient behavior.

There are also some limitations:

- The reset is not "optimized" as it is in the optimum reset method, and a voltage across the primary switcher is higher for the same duty cycle.
- It cannot employ zero voltage-switching features for the main switch unlike the active clamp reset circuit.

Overall, this method offers a simple and low cost solution for the implementation of a forward converter for high efficiency and fast transient response applications.

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