Signal Transfer Through Power Magnetics

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ABSTRACT

This paper presents a method of signal transfer through a power magnetic without interference with the main power train. There will be described two implementations of this concept. In the first application the concept is applied in a 15W DC-DC Converter using flyback topology. The main transformer of the flyback converter is used to store and transfer energy to the secondary and at the same time to transfer the gate signal from the primary side to the secondary side with minimum delay. Incorporating the signal winding and the power winding on the same magnetic core decreases the cost and increases the power density, which is a very important feature for the latest generation of DC-DC Converters.
In the second application of this technology is implemented in a quarter brick DC-DC Converter, using a half bridge topology. In this implementation the gate signal for the primary switchers is transferred from the secondary to primary side through the output chokes. The output chokes are used to store energy and in the same time to transfer signal from the secondary to the primary. The technology is implemented in a DC-DC Converter 132W, 3.3V @ 40A DC-DC Converter, with an efficiency of 91.5% at full load and reaching a power density of 146W/inc3.

INTRODUCTION

In an isolated DC-DC converter using synchronous rectification there are switching elements placed in the primary and switching elements placed in the secondary. The primary and secondary switches are synchronized and the commutations should occur within very small delay time. In the beginning of 1990's the synchronous rectification had favored the selfdriven approach.
Its simplicity wherein the Synchronous rectifiers were driven directly from the transformer windings have played a major role in its popularity. This concept however has some limitations. One of it is the fact that the secondary voltage signal is delayed into the secondary winding by the leakage inductance and this delay is function of the output current.
The turn on can be slightly delayed to prevent cross conduction and the body diode will carry the current for a short period of time. The turn off time is the most critical. An earlier turn off of the synchronous rectifier will force the body diode in conduction leading to reverse recovery losses. A delayed turned off of the synchronous rectifier will lead to cross-conduction because the polarity of the voltage in the secondary will change while the synchronous rectifier is still in conduction.
In the self-driven technology there is a risk that the polarity of the secondary voltage will change before the synchronous rectifier is turned off. This risk is higher for synchronous rectifiers operating at high frequency and high current.
In the driven synchronous rectification technology the signals should be transferred across the isolation boundary quicker than the transformer winding change its polarity.
Gate drive signal from the primary to the secondary can be transferred through a magnetic element. The delay of the signal transfer is function of the leakage inductance, which is proportional to the square of the number of turns. To reduce the number of turns in the magnetic element for signal transfer we have to increase the cross section of the magnetic core, which leads to a larger core size. This is in conflict with the miniaturization and low profile requirements. In addition to that, a magnetic element may require a surface mounted header, which will increase the footprint and will further add to the cost.
The solution proposed in this paper is to use the power magnetic elements such as the transformer or the output inductor for the signal transfer without interference with the main power train.
In figure 2A and 2B is presented a conventional symmetrical winding arrangement, wherein the primary winding and the secondary winding are surrounding the

center leg. When a voltage is applied to the primary winding, there will be a voltage induced in the secondary winding which is the summation of the voltage induced in each outer leg. If V is the voltage induced in each outer leg, the total voltage induced in the secondary winding is 2*V, regardless of the polarity.

In figure 2C and 2D is presented an asymmetrical winding arrangement for the secondary winding. When a voltage is applied to the primary winding the voltage induced in the asymmetrical winding will be the summation of the voltages induced in each outer leg, and because the opposite polarity the total voltage will be zero.

In conclusion the asymmetrical winding does not "see" the voltage induced by the primary winding. If the primary winding and secondary winding of a power transformer is placed in symmetrical winding arrangement, the voltage induced in an asymmetrical winding is zero. This is valid only if the core is perfectly symmetric, and any asymmetry in the E core will lead to an "error" voltage induced in the asymmetrical winding.

In figure 3 is presented the flux through the transformer in a symmetrical and asymmetrical winding arrangement. In a symmetrical winding arrangement the flux links the center leg and closes through the outer leg. If voltage is applied to an asymmetrical winding the flux links the outer legs only and there is not flux through the center leg. It means that no voltage will be induced in a symmetrical winding placed around the center leg.

It can be concluded that two independent signal or power transfers can be performed through an E core. One path is thorough windings wound in a symmetrical structure, and other through windings placed in an asymmetrical structure.

In this paper we will use the asymmetrical winding for the signal transfer and the symmetrical winding for the power transfer. Generally we can use this "two channel" structure for power transfer through two independent regulated outputs, for two independent signal transfer, or a combination of signal and power. It has to be mentioned that the power transfer can be also done though the asymmetrical winding and the symmetrical winding can be used for signal **[13]**.

The flux will add or subtract through the outer legs, an issue which has to be addressed when core loss calculations are performed. In this application we try to minimize the flux swing created by the signal winding.

In figure 4 is presented the circuit used for signal transfer. The gate signal for the primary power switch is applied to A. The square signal is diferentiated by the RC circuit and the resulting waveform B is applied to the primary signal winding which surrounds the outer legs in an asymmetrical configuration. By diferentiating the signal only the information related to the transition are processed, eliminating the lower frequency harmonics and reducing the flux swing in the transformer. The square waveform is reconstructed in the secondary by a pair of PNP and NPN transistors.

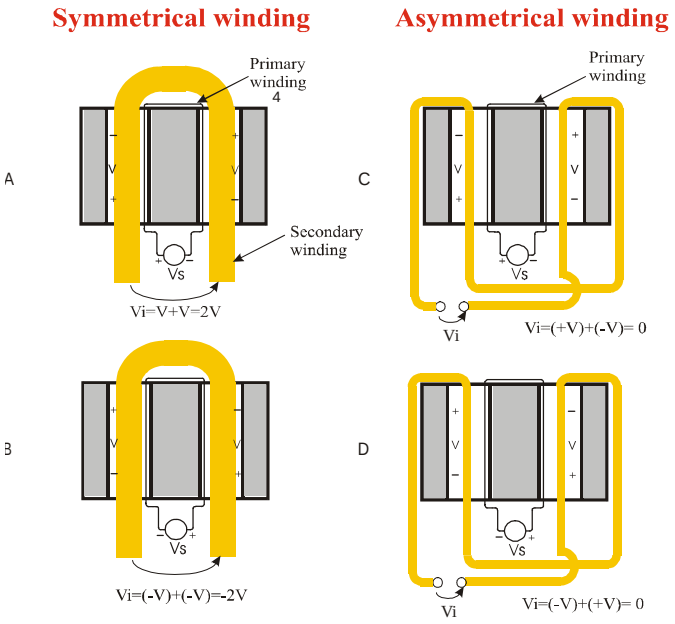


Figure 2

Symmetrical and Asymmetrical winding structure [13]

When the signal in A will have a transition from low to high the PNP transistor will be turned on and the gate capacitance of the synchronous Mosfet will be discharged. When the signal in A has a transition from high to low the NPN transistor will be turned on and the gate of the synchronous rectifier signal will charged.

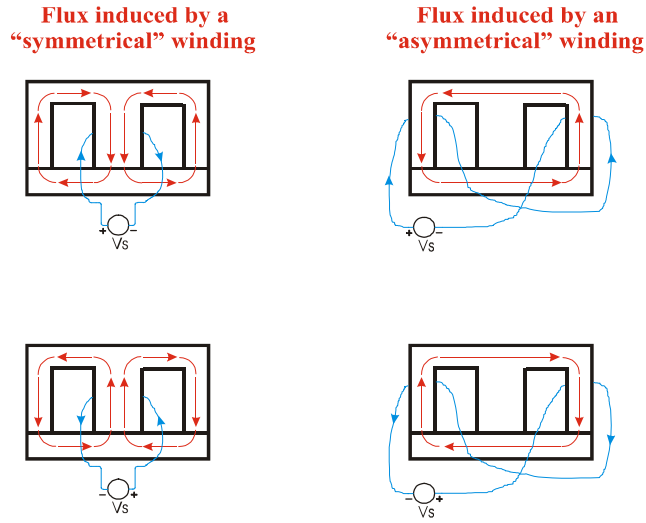


Figure 3

Flux distribution created by a symmetrical and asymmetrical winding [13]

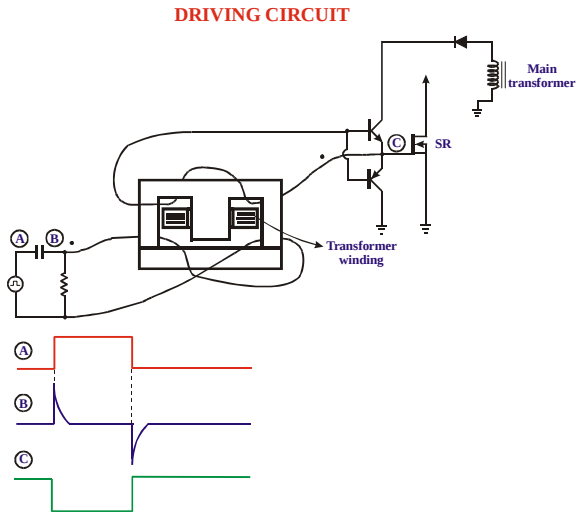


Figure 4

Driving Circuit through the power transformer [13].

In figure 5 is presented the reconstructed gate signal and the voltage drop across the synchronous rectifier. The signal delay in this application was approximately 3ns. This low delay is due to a very low leakage inductance. Using only one turn in primary and one in the secondary leads to a very low leakage inductance for the magnetic element used for the signal transfer. This is an important advantage of this method of signal transfer.

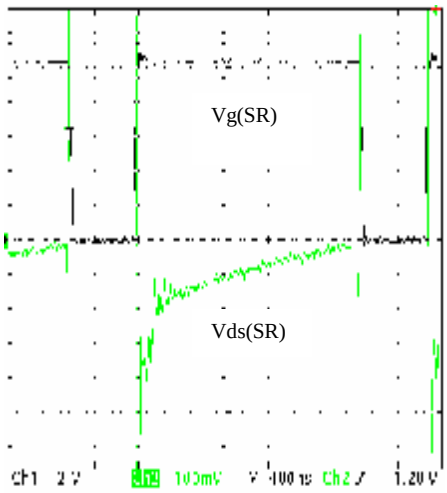


Figure 5

Reconstructed Vg(SR) 2V/div
Voltage across SR 100mV/div

An equivalent discrete magnetic element wherein we can achieve such a low leakage inductance would require a large magnetic core and a large size header. The solution presented in this paper offers a simple solution, which reduces not only the size but also the cost of the converter

IMPLEMENTATION OF THE CONCEPT In a 15W DC-DC CONVERTER

Using this method of signal transfer a 15W, 3.3V @ 4.5A DC-DC Converter operating form an input voltage of 32V to 75V was built and evaluated. The input voltage range is larger than the standard telecom applications, though easy to realize in a flyback topology. The low output voltage and high current is quite a challenge for a flyback topology. To optimize its operation for these specifications the converter was designed to operate at high duty cycle in the secondary, reducing the ratio, peak current versus output current. The transformer is using a planar E18 core and the winding is embelled in a 70um (3oz) multilayers PCB.
There are 8 turns in primary and two turns in the secondary, power windings which are distributed in four layers. The top and the bottom layers of the PCB are used for placing the power and signal components **[11].** The efficiency peaks to 90% at full load.
In figure 7 is presented the simplified schematic and the key waveforms for a continuous mode flyback with synchronous rectification. As is depicted the synchronous rectifier is turned on after the primary switch turns off. There is a delay time in between referred as Tdon. The synchronous rectifier is further turned off before the main switch is turned on with a delay referred as Tdoff. We can identify four stages of operation for the synchronous rectifier.

STAGE 1 (to-t1)

At the moment to, the primary power switch SW is turned off and the magnetizing current will flow into the secondary winding, initially through the body diode, Dsr of the Synchronous Rectifier. During the conduction time of the body diode the voltage drop on the rectifier is larger and as a result during this time interval there is higher power dissipation. One of the designs goals is to minimize the to-t1 time interval.

STAGE 2 (t1-t2)

At the moment t1, the synchronous rectifier is turned on and the voltage drop will decrease as depicted by Vsr(t). By design the voltage drop on the synchronous rectifier has to be much lower than the voltage drop on the Schottky Rectifier. In this particular design as is presented in figure 5, the voltage drop is as low as 50mV, approximately ten

times lower than on a Schottky Diode. During this time interval the power is processed very efficiently.

STAGE 3 (t2-t3)

At the moment t2, the synchronous rectifier is turned off. The current in the secondary will continue to flow through the body diode of SR. During the conduction time of the body diode the voltage drop on the rectifier is larger and as a result the there is higher power dissipation. One of the designs goals is to minimize also the t2-t3 time interval.

STAGE 4 (t3-t4)

At the moment t3, the primary power switch is turned on. Though the synchronous rectifier has been turned off at t2, the current continues to flow through the body diode. At the moment t3, when the primary switch turns on there are still carriers in the junction of the body diode.
When the voltage polarity changes in the secondary as a result of turning on the primary switch, there will be reverse recovery current through the body diode. This will generate two types of losses. First, there are the cross conduction losses on the primary switch due reverse recovery current reflected in the primary. The second type of loss is the reverse recovery losses on the synchronous rectifier.
From the analysis of the stages of the operation is concluded that the minimization of the (to-t1) and (t2-t3) is necessary to improve the performance. To minimize this we have to control the timing accurately. It means that the information about the status of the main switch, sent from the primary side to the secondary side shall be transferred with minimum delay.

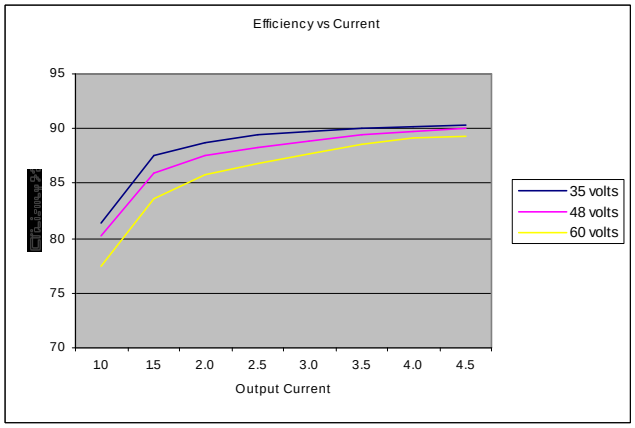


Figure 6
The efficiency versus the output current

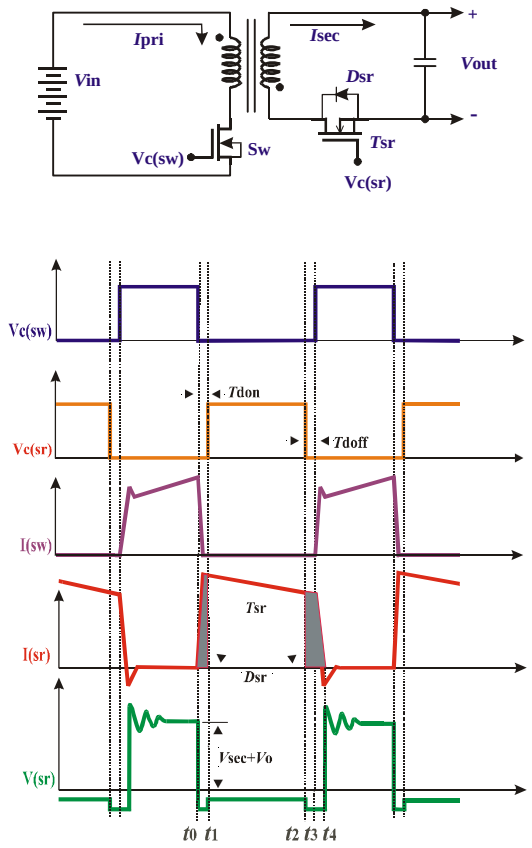


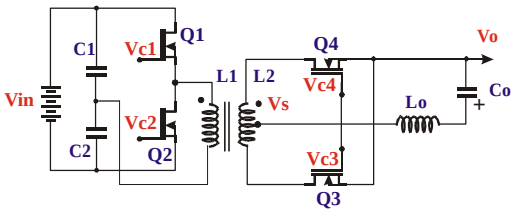
Figure 7

Continuous Mode Flyback with Synchronous Rectification

The high efficiency for relatively low power is a difficult task due to the high ratio of the bias power compared to the output power.

Figure 8
The 15W DC-DC Converter

As can be seen from figure 6 the efficiency decays sharply for output current under 1.5A. The DC-DC Converter is presented in figure 8. A LC output filter is used in order to minimize the output ripple. The peak-to-peak ripple is less than 50mV. The operation frequency of the converter is approximately 350Khz.



Circuit diagram

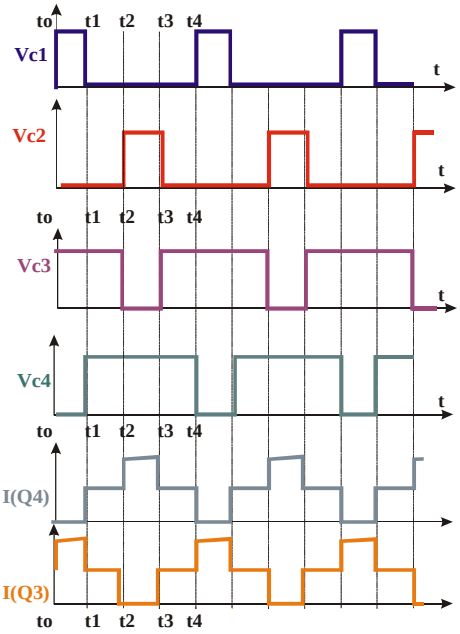
IMPLEMENTATION OF THE CONCEPT
132W DC-DC CONVERTER

Another implementation of this concept was performed in a quarter brick DC-DC Converter 132W, 3.3V @ 40A, with an efficiency of 91.5% at full load and reaching a power density of 146W/inc3. In this implementation the signal was transferred form the secondary to the primary. The converter employs secondary side control and the signals from the PWM controller have to be transferred to the primary side to drive the primary switchers.

In figure 9 is presented the simplified schematic and the key waveforms for a half bridge topology with synchronous rectification. As is depicted, the synchronous rectifiers are turned on during the on time of their equivalent primary switch and they are on together during the dead time. As a result during the dead time the current is split between both synchronous rectifiers and this reduces the voltage drop by half. This is a major advantage of the double-ended topologies with variable dead time in comparison with the rest of topologies in application wherein synchronous rectification are employed.

In order process high current (40A) using thin copper, the output current is split in two by using two transformers and two output inductors. Each section of the power train is processing 20A. In this way we minimize the conduction losses and spread the heat. The outer legs of the output chokes are used to transfer of the signal from the PWM controller to the primary side. In figure 10 is presented the circuit diagram of the converter, which employs this technology.

This driving technique applied to the half bridge topology combines several advantages. The signal transfer delay from the secondary to the primary including the driver is under 10 ns. It offers an efficient, low cost driver for the floating switch SW1. It offers isolation between primary and secondary easily implemented inside of the multiplayer PCB. The secondary side control implementation allows a very fast compensation loop, which inherently leads to outstanding load transient response. The elimination of the optocouplers into the feedback loop increases also the MTBF of the converter. In addition to that it simplifies the circuit and reduces the number of components, which is an important feature in high density DC-DC Converters.



Typical Waveforms

Figure 9

Half Bridge Converter
with Synchronous Rectification

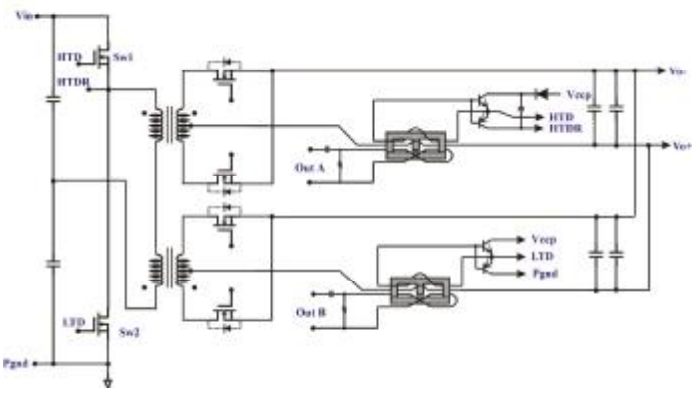


Figure 10
Driving Circuit through the output chokes [13].

In figure 11 is presented the efficiency of the converter versus the load and the input line. The shape of the efficiency versus load underlines the advantage of splitting the power train, which reduces the conduction losses due to a better utilization of the copper [9].
In Figure 12 is presented the implementation of the converter using this full-integrated multilayers PCB [11]. The split of the power train and the distribution of the synchronized rectifiers over the surface of the converter leads to a very efficient thermal distribution.

Figure 11
The efficiency versus the output current

Figure 12
The 146W DC-DC Converter

CONCLUSION

The proposed circuit technique offers the following advantages:

- Eliminates the need for an additional magnetic element for information transfer from primary to secondary, which translates in higher power density and lower cost.
- Improves the utilization of the power magnetic by offering an additional energy or (signal) transfer path without interference with the main power-processing path.
- Using the large cross-section of the power magnetic, the leakage inductance of the signal transfer magnetic element is very low (due to reduced number of turns) and as result there is very low delay time in signal transfer.
- The additional winding complexity in the power magnetic does not add additional cost due to the use of multilayer PCB implementation.

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